REMARKS

Claims 1, 2 and 4-6 are pending after cancellation of the non-elected claims. Claim 6 should now be allowed since it has been rewritten in independent form.

The claims stand rejected under 35 USC §103(a) as being unpatentable over the Prior Art shown by Applicants in Fig. 12 in view of Kollanyi (claim 1) and further in view of Miyazaki et al (claims 2, 4 and 5). Reconsideration of the rejections are respectfully requested.

The Examiner points out that most of the elements of claim 1 are disclosed in Fig. 12 of the drawings in the present application, and both the detecting circuit and the control circuit of claim 1 correspond to element 80 disclosed in Fig. 3 of Kollanyi (4,757,193). Applicants disagree with this interpretation of the reference.

The circuit operation in an optical transmitter may be made unstable by the power on/off operation, causing the power supply voltage to fall and the light emitting diode (LD) to emit the light erroneously. The detecting circuit of the present invention monitors the power supply voltage to detect whether the power supply voltage is lower than a predetermined voltage. The predetermined voltage that is monitored is the threshold of erroneous operation.

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On the other hand, the element 80 disclosed in Fig. 3 of Kollanyi does not monitor the power supply voltage, but monitors the voltage converted from the optical output power. This is obvious from Fig. 4 of Kollanyi. The element 82 (Op-Amp) compares two voltages, one such voltage ((+) marked portion) is the standard voltage relative to the power supply voltage, and the other ((-) marked portion) depends on the optical power of the LASER. Furthermore, transistor 90 of Fig. 4 of Kollanyi has a capacitor at the emitter portion that is connected in series. Accordingly, direct current (DC) cannot flow through the transistor 90 and furthermore cannot continue to cut off a drive current for the ID. Therefore, element 80 of Kollanyi is different from the detecting circuit and the control circuit of claim 1 and the 35 U.S.C. § 103 rejection should be withdrawn.

Further, claims 2, 4 and 5 are dependent claims that set forth additional limitations that are not disclosed or suggested by the art of record. Accordingly each of these claims should be allowed at least for depending from an allowable base claim and further for being patentable over the art of record.

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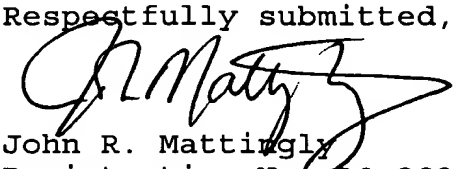
In view of the foregoing amendments and remarks, reconsideration and re-examination are respectfully requested.

Respectfully submitted,



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MARKED UP VERSION OF THE CLAIMS

6. (Amended) [The]An optical transmitter [according to claim 5], for coupling to communication devices though a optical divider/coupler, having a source outputting a drive current, a light-emitting element, for outputting optical signal to an optical fiber coupled to at least one of the communication devices, that is driven by the drive current for generating an optical output signal and, a modulator controlling the supply and cutoff of the drive current to the light-emitting element, comprising:

a detecting circuit that detects a source voltage;

a control circuit that stops, if the detected source voltage is lower than the predetermined voltage, the supply of the drive current to the light-emitting element;

a photodiode that converts part of an optical output signal of the light-emitting element into an electrical signal;

an automatic power control circuit that outputs, in response to the electrical signal from the photodiode, a control signal for making an optical power of the optical output signal constant;

a switch circuit that transmits the control signal outputted from the automatic power control circuit to the

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current source if the detected source voltage is over the predetermined voltage; and

wherein the automatic power control circuit has a buffer circuit that performs level conversion of the light-on/off signal, a first peak hold circuit that holds a maximum output level of the buffer circuit, a second peak hold circuit that holds a maximum output level of the photodiode, and a comparator that makes a comparison between output levels of the first peak hold circuit and the second peak hold circuit.

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